# Tutorial: Germanium as a future channel material for pMOSFETs: Overview of the critical processing steps influencing $I_{on}$ and $I_{off}$

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Ge has emerged as a promising candidate to replace Si for future pMOS devices thanks to its higher hole mobility. In the past years, research reported in literature on germanium focussed on essentially two routes, using Ge either to form a quantum well in a Si substrate, or using Ge as a surface channel material(1). At IMEC, the focus has been on the latter approach, using a Si-compatible process flow(2). The aim of this tutorial is to provide insight in the critical processing steps influencing $I_{on}$ and $I_{off}$ in such an approach, and to give an update on the state of the art at IMEC with respect to these steps.

We start with a global overview of the processing flow currently used at IMEC(3)(Fig. 1). Focussing then on $I_{on}$, we note that high on-currents require high effective channel mobilities and, for short channel devices, a low contribution of the source/drain and contact regions to the series resistance. For a surface channel, the mobility is mainly limited by the passivation of the interface between channel and high-k gate dielectric. We give an overview of the different passivation schemes investigated at IMEC, with some elaboration on the most succesful approach to date for pFET, that using a thin strained epitaxial Si film (Fig. 2). The effect of post metallization anneals with $H_2$ and/or $N_2$ in this scheme will also be discussed. Concerning the reduction in series resistance, we first demonstrate that a significant reduction of the contact resistance can be obtained using a Ni-germanide combined with a TiN/Ti/Al backend metallization stack. We discuss in detail the processing challenges involved with the germanidation and metallization, and explain what principles guided our choice of materials. In order to obtain a low active area resistance, the importance of a pre-amorphisation implant is highlighted and demonstrated. Elaborating somewhat further on dopant behavior, we discuss the remarkable diffusion characteristics of P in Ge, which set the upper limit for the doping level of the P-halos used in our devices to limit short channel effects.

Turning to $I_{off}$, the focus is on perimeter and junction leakage. For both components, we show that the leakage current can be minimized by changing the n-well dose to obtain an optimal junction depletion width. This depletion width should be narrow enough to minimize current generation from the traps and/or interface states inside the depletion layer, but on the other hand wide enough to minimize band-to-band and trap assisted tunneling(4) (Fig. 3). Special attention is given in this section to the impact on leakage of the high threading dislocation density, present when using Ge on Si substrates.

We conclude with a short overview of the main future directions and challenges, where the emphasis will be on the implementation of compressively strained Ge on SiGe (Fig. 4) to further enhance channel mobility.

(1) See e.g. S.W. Bedell *et al.*, Materials Science in Semiconductor Processing 9 (2006) pp. 423-436
(2) P. Zimmerman *et al.*, IEDM Tech. Digest (IEEE, Piscataway, 2006), p. 655
(3) For a detailed overview on all process steps, see D. Brunco *et al.*, proceedings of the MRS fall (2007), and references therein
(4) G. Eneman *et al.*, submitted to IEEE Transactions, Electron Devices

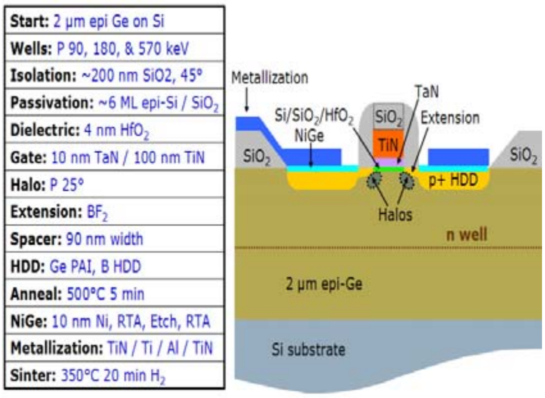


Fig. 1: Overview of processing steps in the IMEC pMOS flow (ref 2).

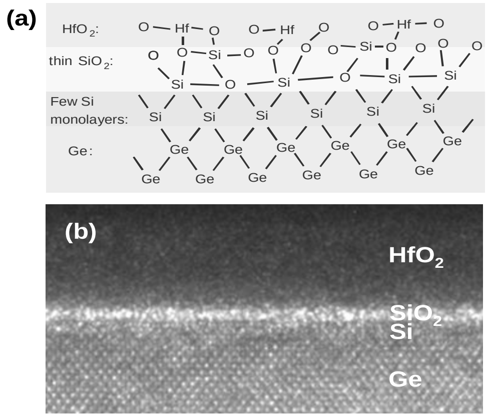


Fig. 2: TEM and schematic of the Si-passivation technique.

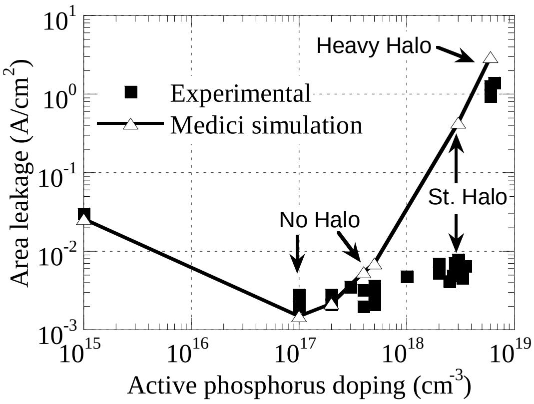


Fig.3: Comparison of experimental data for area leakage with simulation results using Tsuprem and Medici (ref. 4). The results show a minimum around 1e17-5e17/cm$^3$.

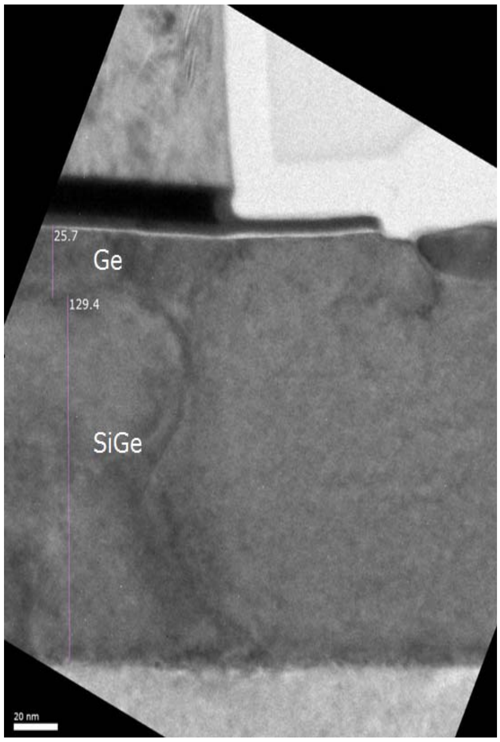


Fig. 4: TEM of 25nm strained Ge on 130nm $Si_{0.2}Ge_{0.8}$