Yesterday, Today, and Tomorrow of High-K/Metal Gated Devices

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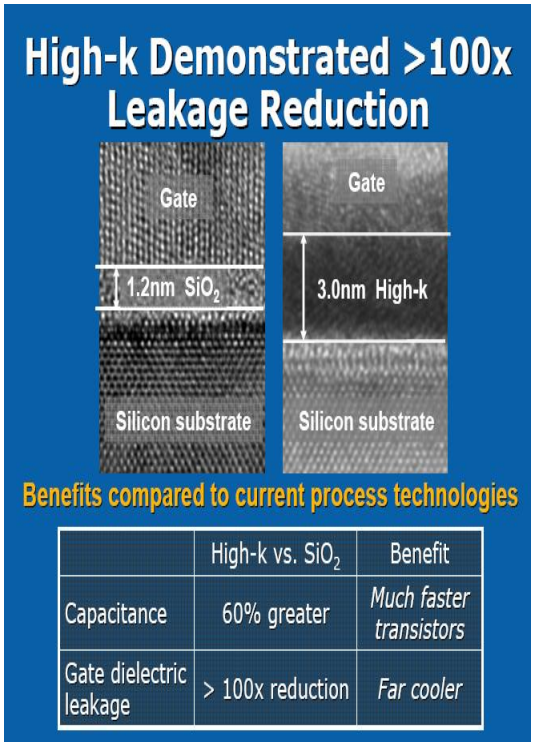
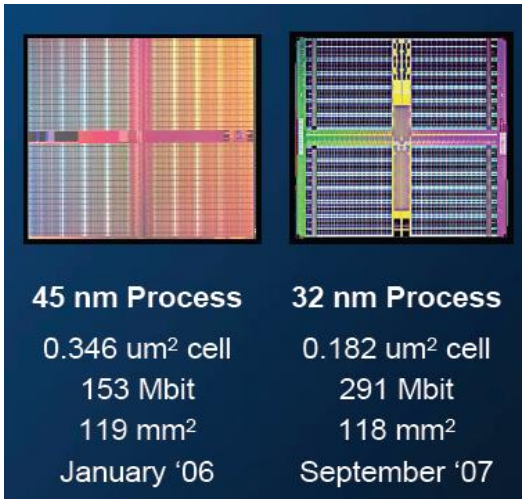
This short course covers three parts: (1) Research and development of early High-K/Metal Gate devices. The historical perspective helps the audience understand why and how the options were narrowed down to current gate stack. The current choice may not be the best one to meet the future needs. (2) Introduce the High-K/Metal Gate stack materials and the process integration options for current technology nodes including the threshold voltage control. (3) The challenges of future High-K/Metal Gate devices beyond 32 nm technology node including the equivalent oxide thickness (EOT) scaling. Also shown is the impact of the quality of the SiO2/Si interface on the ultra-thin High-K/Metal Gate MOSFET reliability and threshold voltage- EOT roll-off. Finally, techniques to improve the interface quality of a High-K/Metal Gate stack will be discussed.

- **Yesterday: 10-year R&D efforts**

- **Today: 1st (45 nm) and 2nd (32 nm) Generation High-K**



	High-k vs. SiO_2	Benefit
Capacitance	60% greater	*Much faster transistors*
Gate dielectric leakage	> 100x reduction	*Far cooler*



Intel SRAM test chips
(www.intel.com)

- **Tomorrow: High-K/Metal Gate beyond 32 nm technology node = ?**

"Learn from yesterday, live for today, hope for tomorrow. The important thing is not to stop questioning." - Albert Einstein